Amendments To The Specification:

Please replace paragraph **[0025]** with the following amended paragraph:

[0025] ~~Even for a link whose link rate (which is the serial link bit rate / 10 for a link that uses 10 bit character such as 8B/10B characters) may be different from the pixel clock rate, there is a benefit in defining the link rate with these four parameters, A', B', C', and D': The benefit is the simplicity in regenerating pixel/audio clocks from a link clock. For example, let's say the link rate is set as A' = 6, B' = 3, C' = 7, and D' = 0 (i.e., LR = 2^6 x 3^3 x 5^7 x 11^0) and the corresponding link rate is 135MHz. However, suppose the pixel clock rate is set as A = 8, B = 3, C = 6, and D = 0 (i.e., PC = 2^8 x 3^3 x 5^6 x 11^0) and the corresponding pixel clock rate is 108MHz, then the pixel clock can be generated from link clock by the following equation~~

~~Pixel clock rate = (link rate) x ($2^{A-A'}$, $3^{B-B'}$, $5^{C-C'}$, and $11^{D-D'}$). For the above example, (Pixel clock rate/Link rate) = (2^8 x 3^3 x 5^6 x 11^0)/ (2^6 x 3^3 x 5^7 x 11^0) or~~

~~Pixel clock rate = (Link rate) x (2^2)x(3^0)x(5^{-1})x(11^0) = Link rate x (.8).~~

In the described embodiment, a main link data rate is chosen whose bandwidth exceeds the aggregate bandwidth of the constituent virtual links. Data sent to the interface arrives at the transmitter at its native rate. A time-base recovery (TBR) unit 226 within the receiver 104 regenerates the stream's original native rate using time stamps embedded in the main link data packets, if necessary. It should be noted, however, that for appropriately configured digital display devices 232 shown in Fig. 2B, time base recovery is unnecessary since display data is be sent to the display driver electronics at the link character clock rate, thereby greatly reducing the number of channels required with a commensurate reduction in complexity and cost for the display. For example, Fig. 2C illustrates an exemplary LCD panel 232 configured in such a way that no time base recovery since display data is essentially pipelined to the various column

drivers 234 that are used in combination with row drivers 236 to drive selected display elements 238 in the array 240.

Please replace paragraph **[0027]** with the following amended paragraph:

[0027] Even for a link whose link rate (which is the serial link bit rate / 10 for a link that uses 10-bit character such as 8B/10B characters) may be different from the pixel clock rate, there is a benefit in defining the link rate with these four parameters, A', B', C', and D': The benefit is the simplicity in regenerating pixel/audio clocks from a link clock. For example, let's say the link rate is set as A' = 6, B' = 3, C' = 7, and D' = 0 (i.e., LR = $2^6 \times 3^3 \times 5^7 \times 11^0$) and the corresponding link rate is 135MHz. However, suppose the pixel clock rate is set as A = 8, B = 3, C = 6, and D = 0 (i.e., PC = $2^8 \times 3^3 \times 5^6 \times 11^0$) ~~(=~~ and the corresponding pixel clock rate is 108MHz~~)~~, then the pixel clock can be generated from link clock by the following equation

Pixel clock rate = (link rate) x ($2^{A-A'}$, $3^{B-B'}$, $5^{C-C'}$, and $11^{D-D'}$). For the above example,

(Pixel clock rate/Link rate) = $(2^8 \times 3^3 \times 5^6 \times 11^0)/(2^6 \times 3^3 \times 5^7 \times 11^0)$ or

Pixel clock rate = (Link rate) x $(2^2)x(3^0)x(5^{-1})x(11^0)$ = Link rate x (.8).

~~as pixel clock rate is equal to the link rate * 22 / 51 .~~